WHAT IS CLAIMED IS:

1. A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

said processing unit and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

2. The microprocessor integrated circuit of claim 71 wherein said memory is dynamic random-access memory.

3. The microprocessor integrated circuit of claim 71 wherein said memory is static random-access memory.

4. A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions; and

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate.

5. The microprocessor integrated circuit of claim 74 wherein said memory is dynamic-access memory.

6. The microprocessor integrated circuit of claim 74 wherein said memory is static random-access memory.

7. The microprocessor integrated circuit of claim 74 wherein said memory is capable of supporting read and write operations.

8. microprocessor integrated circuit comprising:

a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed upon a substrate; and

a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate.

9. he microprocessor integrated circuit of claim 78 wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.

10. he microprocessor integrated circuit of claim 78 further including memory controller means coupled to said memory for performing direct memory access data transfer through said one or more interface ports.

11. A multiprocessor computational system comprising:

a first processing unit and a first memory disposed upon a first substrate and coupled to said processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. The system of claim 81 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. The multiprocessor system of claim 81 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.